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CENTRAL FAX CENTERSerial No.: 10/675,432
Accompanying Amendment

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Docket No. 1001.29
Customer No. 53953Amendments to the Claims

The following listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Currently amended) A method of reducing power consumption in an N -way set-associative cache memory having Y sets, wherein N is a first integer, and wherein Y is a second integer, the method comprising:

 during a first clock cycle k , in response to a first address, identifying a first associated set in the cache memory, comparing the first address to respective tag portions of N blocks in the first associated set, and outputting a first signal in response thereto, wherein k is an integer; and

during a second clock cycle $k+1$, in response to the first signal indicating that one of the N blocks in the first associated set is a match with the first address, enabling reading a respective non-tag portion of the matching block in the first associated set, while non-tag portions of $N-1$ non-matching blocks in the associated set are disabled, and while non-tag portions of $Y-1$ non-associated sets are disabled;

during a second clock cycle $k+1$, in response to the first signal indicating that one of the N blocks in the first associated set is a match with the first address, reading the enabled non-tag portion of the matching block in the first associated set;

during the second clock cycle $k+1$, in response to a second address, identifying a second associated set in the cache memory, comparing the second address to respective tag portions of N blocks in the second associated set, and outputting a second signal in response thereto; and

in response to the second signal indicating that one of the N blocks in the second associated set is a match with the second address, enabling a respective non-tag portion of the matching block in the second associated set instead of the respective non-tag portion of the matching block in the first associated set.

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2. (Currently amended) The method of Claim 1, wherein the reading the enabled non-tag portion of the matching block in the first associated set comprises:

reading enabling the enabled non-tag portion of the matching block in the first associated set, while respective non-tag portions of N-1 non-matching blocks in the first associated set are at least partly disabled, and while respective non-tag portions of Y-1 non-associated sets are at least partly disabled.

3. (Currently amended) The method of Claim 1-2, wherein the enabling the respective non-tag portion of the matching block in the first associated set comprises:

applying power to the respective non-tag portion of the matching block in the first associated set.

4. (Currently amended) The method of Claim 2-4, and comprising:

removing power from at least one of the respective non-tag portions of: the N-1 non-matching blocks in the first associated set; and the Y-1 non-associated sets.

5. (Currently amended) The method of Claim 4, wherein the removing power from the respective non-tag portions comprises:

removing power from the at least one of the respective non-tag portions, so that the respective non-tag portions are disabled from outputting information, and so that the respective non-tag portions continue to store the information.

6. (Previously presented) The method of Claim 1, wherein the cache memory is a program cache.

7. (Previously presented) The method of Claim 1, wherein the cache memory is a data cache.

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8. (Currently amended) The method of Claim 1, wherein the comparing the first address to respective tag portions of N blocks in the first associated set comprises:
comparing a portion of the first address to the respective tag portions of the N blocks in the first associated set.

9. (Currently amended) The method of Claim 1, wherein comparing the first address to respective tag portions of N blocks in the first associated set the reading comprises:

comparing the first address to the respective tag portions of N blocks in the first associated set, while reading the non-tag portion of the matching block in the associated set, while the respective non-tag portions of the N-1 non-matching blocks in the first associated set are at least partly disabled, and while respective the non-tag portions of the Y-1 non-associated sets are at least partly disabled.

10. (Currently amended) The method of Claim 1, and comprising:
during the second clock cycle k+1, in response to a second address, identifying a second associated set in the cache memory, comparing the second address to respective tag portions of N blocks in the second associated set, and outputting a second signal in response thereto; and

during a third clock cycle k+2, in response to the second signal indicating that one of the N blocks in the second associated set is a match with the second address, reading the enabled a non-tag portion of the matching block in the second associated set, while non-tag portions of N-1 non-matching blocks in the second associated set are disabled, and while non-tag portions of Y-1 non-associated sets are disabled.

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11. (Currently amended) A system for reducing power consumption in an N -way set-associative cache memory having Y sets, wherein N is a first integer, and wherein Y is a second integer, the system comprising:

first circuitry for: during a first clock cycle k , in response to a first an-address, identifying a first an-associated set in the cache memory, comparing the first address to respective tag portions of N blocks in the first associated set, and outputting a first signal in response thereto, wherein k is an integer; and

second circuitry for: ~~during a second clock cycle $k+1$, in response to the first signal indicating that one of the N blocks in the first associated set is a match with the first address, enabling reading a respective non-tag portion of the matching block in the first associated set, while non-tag portions of $N-1$ non-matching blocks in the associated set are disabled, and while non-tag portions of $Y-1$ non-associated sets are disabled;~~

third circuitry for: during a second clock cycle $k+1$, in response to the first signal indicating that one of the N blocks in the first associated set is a match with the first address, reading the enabled non-tag portion of the matching block in the first associated set;

wherein the first circuitry is for: during the second clock cycle $k+1$, in response to a second address, identifying a second associated set in the cache memory, comparing the second address to respective tag portions of N blocks in the second associated set, and outputting a second signal in response thereto; and

wherein the second circuitry is for: in response to the second signal indicating that one of the N blocks in the second associated set is a match with the second address, enabling a respective non-tag portion of the matching block in the second associated set instead of the respective non-tag portion of the matching block in the first associated set.

12. (Currently amended) The system of Claim 11, wherein the third second circuitry is for reading enabling the enabled non-tag portion of the matching block in the first associated set, while respective non-tag portions of $N-1$ non-matching blocks in the first associated set are at least partly disabled, and while respective non-tag portions of $Y-1$ non-associated sets are at least partly disabled.

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13. (Currently amended) The system of Claim 11-12, wherein the second circuitry is for applying power to the respective non-tag portion of the matching block in the first associated set.

14. (Currently amended) The system of Claim 12-11, wherein the second circuitry is for removing power from at least one of the respective non-tag portions of: the N -1 non-matching blocks in the first associated sets, and the Y -1 non-associated sets.

15. (Currently amended) The system of Claim 14, wherein the second circuitry is for removing power from the at least one of the respective non-tag portions, so that the respective non-tag portions are it is disabled from outputting information, and so that the respective non-tag portions continue it continues to store the information.

16. (Previously presented) The system of Claim 11, wherein the cache memory is a program cache.

17. (Previously presented) The system of Claim 11, wherein the cache memory is a data cache.

18. (Currently amended) The system of Claim 11, wherein the first circuitry is for comparing a portion of the first address to the respective tag portions of the N blocks in the first associated set.

19. (Currently amended) The system of Claim 11, wherein the first second circuitry is for comparing the first address to the respective tag portions of N blocks in the first associated set, while reading the non-tag portion of the matching block in the associated set, while the respective non-tag portions of the N-1 non-matching blocks in the first associated set are at least partly disabled, and while respective the non-tag portions of the Y -1 non-associated sets are at least partly disabled.

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20. (Currently amended) The system of Claim 11, wherein:

~~the first circuitry is for: during the second clock cycle $k+1$, in response to a second address, identifying a second associated set in the cache memory, comparing the second address to respective tag portions of N blocks in the second associated set, and outputting a second signal in response thereto; and~~

~~the third second-circuitry is for: during a third clock cycle $k+2$, in response to the second signal indicating that one of the N blocks in the second associated set is a match with the second address, reading the enabled a non-tag portion of the matching block in the second associated set, while non-tag portions of $N-1$ non-matching blocks in the second associated set are disabled, and while non-tag portions of $Y-1$ non-associated sets are disabled.~~